REMARKS/ARGUMENTS

Favorable reconsideration of this application as presently amended and in light of the following discussion is respectfully requested.

Claims 1-2, 18-19 and 22-31 are presently active in this case, Claims 3-17 and 20-21 have been canceled without prejudice, and Claims 1 and 26 are amended. No new matter is added.

In the outstanding Official Action, Claims 1, 2, 18, 19 and 22-25 were objected to because of informalities; Claims 1, 2, 22-24, 26 and 28-30 were rejected under 35 U.S.C. 103(a) as unpatentable over Gerber et al. (U.S. Patent No. 5,401,913) in view of either one of Bohn (U.S. Patent No. 6,537,412) or Johnston (U.S. Patent No. 5,153,050) and Daigle et al., Enomoto et al. (WO 98/56220), and optionally Fukukawa (JP 08-293677); Claims 18, 19 and 27 were rejected under 35 U.S.C. 103(a) as unpatentable over Gerber et al., either one of Bohn or Johnston and Daigle et al., Enomoto et al., and optionally Fukukawa, and further in view of Kimura et al. (U.S. Patent No. 6,376,782); Claims 25 and 31 were rejected under 35 U.S.C. 103(a) as unpatentable over Gerber et al., either one of Bohn or Johnston and Daigle et al., Enomoto et al., and optionally Fukukawa, and further in view of Reavill et al. (U.S. Patent No. 4,290,838).

Regarding the objection to the claims, Claim 1 is amended as suggested by the outstanding Office Action. Thus, it is respectfully submitted that the objection to the claims is overcome.

Regarding the rejection under 35 U.S.C. 103(a), Applicants respectfully traverse the outstanding grounds for rejection, because in Applicants' view, independent Claim 1 patentably distinguishes over the applied references as discussed below.

Claim 1 recites, *inter alia*, "***integrating the second printed board, the printed board with the conductor circuit, and the outermost copper foil by heating and one time of pressing*** such that the conductive bump in each printed board pierces through the

corresponding bonding layer covering the conductive bump and is electrically connected to corresponding one of the conductor circuit and the outermost copper foil" and "thereafter, ***etching the outermost copper foil*** and the copper foil on opposite surfaces of the integrated printed boards so as to form conductive circuits, thereby obtaining the multilayer circuit board." Thus, Claim 1 recites, *inter alia*, integrating a printed board, a printed board with a conductor circuit and an outermost copper foil, which is etched so as to form conductive circuits, by heating and one time of pressing.

The outstanding Office Action acknowledges that Gerber et al. does not teach an upper outermost copper conductor layer (Office Action at page 3, lines 15-16). Instead, the outstanding Office Action states that Gerber et al. teaches the multilayer circuit board of Fig. 9 is connected on its upper side to substrates including a copper conductor layer to form an integral, operable multilayer circuit board (Office Action at page 3, lines 16-20). Further, the outstanding Office Action relies on Bohn and Johnston to remedy the deficiencies of Gerber et al., indicating that Bohn and Johnston both disclose placing outermost copper foils covering the entire surface of the outermost printed circuit boards on the stack (Office Action at page 3, line 20 though page 4, line 19).

First, Bohn shows in Fig. 1 a multilayer 1 comprising inner layers 3, intermediate layers 4 and outer foils 2a, 2b. The intermediate layers 4 are impregnated with adhesives, the so-called prepregs (Bohn at col. 1, lines 53-55). The inner layers 3 are connected to the outer foils 2a, 2b with the intermediate layers 4 formed therebetween as adhesives. However, Bohn describes "[i]t is now essential that the metal foils 2a and 2b are not arranged as was customary until now, separately on the upper side and underside of the separation sheet, but instead that a single metal foil 2a, 2b runs through from top to bottom as a single piece, and thus surrounds the separation layer 5 in a U-shape" (Bohn at col. 4, lines 1-6). That is, Bohn does not assume etching the foils 2a, 2b to form conductive circuits. Thus, the foils 2a, 2b

shown in Bohn do not correspond to "the outermost copper foil" as recited in Claim 1, and Bohn does not teach or suggest integrating a printed board, a printed board with a conductor circuit and an outermost copper foil, which is etched so as to form conductive circuits, by heating and one time of pressing.

Next, Johnston shows in Fig. 1 a multilayer comprising a laminated multilayer core 10 and copper foil layers 4. The laminated multilayer core 10 is constituted by laminating prepreg layers 12, boards 14 and conductive paths 15. Johnston describes placing the laminated multilayer core 10 on a sheet of copper foil 4 and placing another sheet of copper foil 4 on the laminated multilayer core 10 (Johnston at col. 4, lines 36-44). However, the copper foil layers 4 are laminated with the laminated multilayer core 10, in which the prepreg layers 12, the boards 14 and the conductive paths 15 have been already laminated. Thus, Johnston does not teach or suggest integrating the prepreg layers 12, the boards 14, the conductive paths 15 and the copper foil layers 4 by heating and one time of pressing. Therefore, the copper coil layers 4 do not correspond to "the outermost copper foil" as recited in Claim 1, and Johnston does not teach or suggest integrating a printed board, a printed board with a conductor circuit and an outermost copper foil, which is etched so as to form conductive circuits, by heating and one time of pressing.

Likewise, Daigle et al., Enomoto et al. and Fukukawa also fail to teach or suggest the features above as recited in Claim 1.

Accordingly, the applied references fail to teach or suggest at least "integrating the second printed board, the printed board with the conductor circuit, and the outermost copper foil by heating and one time of pressing such that the conductive bump in each printed board pierces through the corresponding bonding layer covering the conductive bump and is electrically connected to corresponding one of the conductor circuit and the outermost copper foil" and "thereafter, etching the outermost copper foil and the copper foil on opposite

surfaces of the integrated printed boards so as to form conductive circuits, thereby obtaining the multilayer circuit board," as recited in Claim 1.

Similar arguments as set forth above also apply to Claim 26.

Thus, independent Claims 1 and 26 patentably distinguish over the applied references. Since Claims 2, 18, 19, 22-25 and 27-31 are dependent directly or indirectly from Claims 1 and 26, substantially the same arguments set forth above also apply to these dependent claims. Therefore, Claims 18-19 and 22-31 are believed to be allowable.

In view of the amendments and discussions presented above, Applicant respectfully submits that the present application is in condition for allowance, and an early action favorable to that effect is earnestly solicited.

Respectfully submitted,

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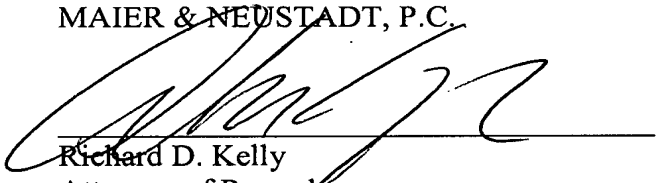

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